

Methods Of Forming A Conductive Line, And Integrated Circuitry

TECHNICAL FIELD

This invention relates to methods of forming conductive lines, and to integrated circuitry.

BACKGROUND OF THE INVENTION

The reduction in memory cell and other circuit size implemented in high density dynamic random access memories (DRAMs), static random access memories (SRAMs), logic and other circuitry is a continuing goal in semiconductor fabrication. Implementing electric circuits involves connecting isolated devices through specific electric paths. When fabricating silicon and other semiconductive materials into integrated circuits, conductor devices built into semiconductive substrates need to be isolated from one another. Such isolation typically occurs in the form of LOCOS grown field oxide, and more recently in isolation trench and refill field isolation regions.

Conductive lines, for example transistor gate lines, are formed over substrates. Some lines run globally over large areas of the substrate. Others are much shorter and associated with very small portions of the integrated circuitry. This invention was principally motivated in making processing and structural improvements involving local interconnects.

SUMMARY

The invention includes methods of forming conductive lines, and integrated circuitry. In but one implementation, a method of forming a local interconnect includes forming an isolation trench within a semiconductor substrate. A first trench isolation material is deposited over the semiconductor substrate and to within the isolation trench. First trench isolation material is removed effective to form a line trench within the isolation material into a desired local interconnect configuration. Conductive material is formed within the line trench. A second trench isolation material is deposited over the first trench isolation material, over the conductive material within the isolation trench and within the line trench. At least some first and second trench isolation material is removed from the substrate in at least one common removing step.

In one implementation, a method of forming a local interconnect includes providing a bulk semiconductor substrate having a first conductivity type background region, an adjacent second conductivity type background region and a boundary extending therebetween. An isolation trench is formed within the bulk semiconductor substrate over and along the boundary. A trench isolation material is deposited over the bulk semiconductor substrate and to within the isolation trench. Trench isolation is removed effective to form a line trench within the isolation material into a desired local interconnect configuration. Conductive material is formed to within the line trench.

In one implementation, integrated circuitry includes a semiconductor substrate comprising trench isolation material. A local interconnect line is

received within a trench formed within the trench isolation material. The local interconnect line includes at least two different conductive materials. One of the conductive materials lines the trench. Another of the conductive materials is received within a conductive trench formed by the one.

Other implementations and aspects are contemplated.

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BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a schematic of exemplary integrated circuitry.

Fig. 2 is a diagrammatic sectional view of a semiconductor wafer fragment in process in accordance with an aspect of the invention.

Fig. 3 is a view of the Fig. 2 wafer fragment at a processing step subsequent to that shown by Fig. 2.

Fig. 4 is a view of the Fig. 3 wafer fragment at a processing step subsequent to that shown by Fig. 3.

Fig. 5 is a view of the Fig. 4 wafer fragment at a processing step subsequent to that shown by Fig. 4.

Fig. 6 is a top plan view of a larger portion of the wafer fragment in process, the above fragmentary views being taken through line X-X in Fig. 6.

Fig. 7 is a view of the Fig. 5 wafer fragment at a processing step subsequent to that shown by Fig. 5.

Fig. 8 is a view of the Fig. 7 wafer fragment at a processing step subsequent to that shown by Fig. 7.

Fig. 9 is a view of the Fig. 8 wafer fragment at a processing step subsequent to that shown by Fig. 8.

Fig. 10 is a view of the Fig. 9 wafer fragment at a processing step subsequent to that shown by Fig. 9.

Fig. 11 is a top plan view like Fig. 6, but shown at a processing step subsequent to that of Figs. 6 and 10.

Fig. 12 is a view of a portion of the Fig. 11 wafer fragment as taken through line 12-12 in Fig. 11.

Fig. 13 is a view of the Fig. 12 wafer fragment at a processing step subsequent to that shown by Fig. 12.

FIG. 11

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

The invention contemplates methods of forming local interconnects, and any integrated circuitry involving a local interconnect line, in accordance with the literal wording of the claims. The invention is described with respect to but one exemplary integrated circuit shown in Fig. 1. Such depicts a cross-coupled inverter circuitry 10 comprising n-type transistors T1n and T2n, and p-type transistors T3p and T4p. A local interconnect LI interconnects the gates of T2n and T4p with source/drain regions of T1n and T3p.

Referring to Fig. 2, a semiconductor wafer fragment is indicated generally with reference 12. Such comprises a bulk semiconductor substrate having a first conductivity-type background region 16 adjacent a second conductivity-type background region 18, and a boundary 20 extending therebetween. An exemplary preferred material for bulk substrate 14 is monocrystalline, for example monocrystalline silicon, with region 16 being shown lightly background doped with "n" type impurity and region 18 being lightly background doped with "p" type impurity. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either

alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. Also in the context of this document, the terms "layer" and "material" encompass both the singular and the plural unless otherwise indicated. A pad oxide layer 22 is formed over bulk substrate 14. An exemplary thickness is 100 Angstroms. A masking layer 24 is formed over layer 22. An exemplary material is silicon nitride deposited to an exemplary thickness of 900 Angstroms.

Referring to Fig. 3, an isolation trench 26 is formed within bulk semiconductor substrate material 14, which is laterally centered and extends along p-type/n-type boundary 20. Such will be utilized to form interwell isolation, with an exemplary open width of depicted trench 26 being about 0.5 micron. An exemplary depth within substrate material 14 is 3000 Angstroms. Such provides but one example of forming an isolation trench within a semiconductor substrate. Further in the depicted and preferred embodiment, the isolation trench is formed in bulk substrate material, although the invention is in no way so limited. For purposes of the continuing discussion, isolation trench 26 can be considered as having opposing longitudinal sidewalls 25 in the depicted cross-section. Further in the depicted embodiment, isolation trench 26 is formed to be laterally centered over boundary 20.

Referring to Fig. 4, a first trench isolation material 28 is deposited over substrate 14 and within isolation trench 26. A preferred method of forming layer 28 is by high density plasma chemical vapor deposition. Sidewalls 25 of

trench 26 are preferably thermally oxidized (not shown) before or after deposition of material 28.

Referring to Figs. 5 and 6, exemplary active areas 34 can be seen. First trench isolation material 28 is removed effective to form a line trench 30 within the isolation material into a desired local interconnect configuration. Such removing preferably comprises photolithography and chemical etching, and forms at least a portion of line trench 30 to be laterally centered within isolation trench 26 between sidewalls 25, and laterally centered over boundary 20. In the preferred embodiment, Fig. 6 depicts that line trench 30 includes extensions 32 which do not extend to an edge of the trench isolation material proximate active area substrate material/regions 34. Accordingly at this point in the process in the preferred embodiment, local interconnect trench 30 does not extend to connect with the illustrated active areas. Fig. 6 also depicts exemplary transistor gate outlines 36, which would typically not be formed at this point in the preferred embodiment process. Regardless, it can be seen that the far right illustrated edge of local interconnect trench 30 is also spaced from, and therefore does not connect with, the right illustrated transistor gate outline 36, in this preferred embodiment.

Conductive material is formed within trench 30 to form at least a portion of the local interconnect being formed. Fig. 7 illustrates but one exemplary embodiment wherein a first conductive material 40 is formed, preferably by depositing, to within trench 30 to form a conductive lining therewithin. In one preferred embodiment, layer 40 is formed of an oxidation resistant material.

Exemplary materials include tungsten silicide and nitrogen-rich titanium nitride. In such preferred embodiment, such thereby forms an oxidation resistant lining within line trench 30. In an alternate considered embodiment, the oxidation resistant liner material might be insulative as opposed to conductive. An exemplary insulative oxidation resistant liner material is silicon nitride. A second conductive material 42, different from first conductive material 40, is deposited to within line trench 30 on (in contact with) conductive lining 40. Exemplary materials for layer 42 include tungsten and doped polysilicon. Of course, a single conductive material could be utilized or more than two conductive materials utilized.

Referring to Fig. 8, conductive materials 40/42 are recessed within line trench 30 after their deposition. An exemplary preferred process for doing so would be one or more suitable timed chemical etching(s). Such provides but a few preferred examples of forming conductive materials to within line trench 30.

Referring to Fig. 9, a second trench isolation material 46 is deposited over first trench isolation material 28, over recessed conductive material 40/42 within isolation trench 26, and within line trench 30. Second trench isolation material 46 might be the same composition as first trench isolation material 28, or be of different composition. More preferably, such are the same material, with high density plasma deposited oxide being the preferred example. In the illustrated and preferred embodiment, second trench isolation material 46 is formed on (in contact with) conductive materials 40/42.

Referring to Fig. 10, at least some first trench isolation material 28 and at least some second trench isolation material 46 are removed from the substrate in at least one common removing step. A preferred process includes chemical mechanical polishing (CMP). In the depicted preferred embodiment, such polishing is shown conducted effective to substantially stop on nitride masking layer 24. Of course, polishing could also be continued to remove more material, for example polishing through nitride layer 24 and pad oxide layer 22. Further by way of example only, nitride layer 24 and pad oxide layer 22 might be selectively chemically etched in processing subsequent to that depicted by Fig. 10.

Referring to Figs. 11 and 12, an insulative material 50 is formed over trench isolation material 28/46 and over conductive material 40/42. Exemplary materials for layer 50 include undoped and doped oxides, for example borophosphosilicate glass, phosphosilicate glass, and other doped and undoped silicon dioxides. Further at this point in the process, gate lines 36 have been fabricated prior to deposition of layer 50, and layers 24 and 22 have been removed. Contact openings 52 are etched into insulative material 50 to bridge over and between active area substrate material 34 and conductive material 40/42 within line trench 30.

Referring to Fig. 13, a conductor is formed within contact openings 52 which electrically connects the conductive material with the active area substrate material, and with the far right illustrated gate 52 as shown in Fig. 6. Such

thereby effectively extends the conductive local interconnect line to electrically connect with the depicted source/drain regions and transistor gate line.

The invention also contemplates integrated circuitry comprising a local interconnect line independent of any method of fabrication.

The invention may have particular application in the formation of local interconnects in the periphery of SRAM circuitry. Processing and circuitry in accordance with the invention can serve to provide an extra level of interconnect, thereby freeing up space for higher level interconnects at upper levels of the fabrication. By embedding an extra level of interconnect in trench isolation areas, tighter metallization and interconnect density might be achievable.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.